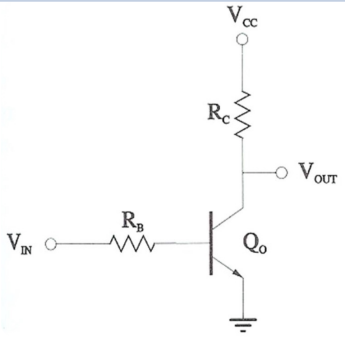
Chapter 5: Resistor Transistor Logic

Basic RTL Inverter

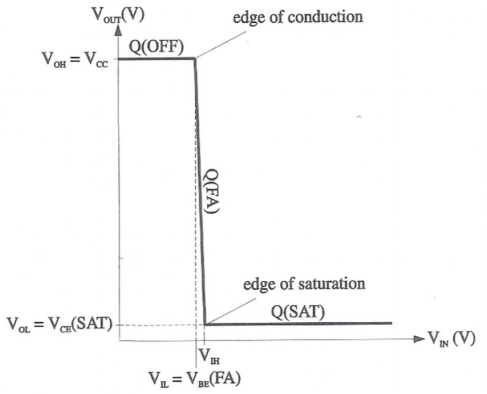


$V_{OH} = V_{CC}$

$V_{IL} = V_{BE(FA)}$

$V_{OL} = V_{CE(sat)}$

$$V_{IH} = V_{BE(sat)} + \frac{V_{CC} - V_{CE(sat)}}{\beta_f R_C} R_B$$

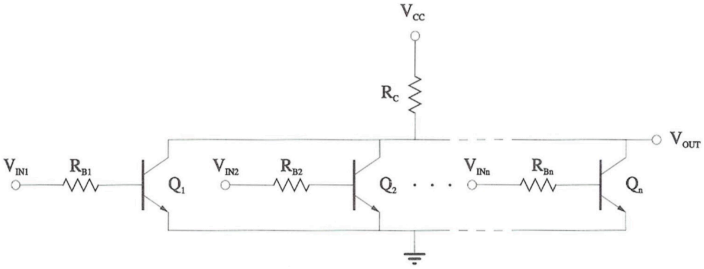


Basic RTL NOR Gate.

*the current through the single collector resistor is the sum of the BJT collector currents

$$I_{RC} = \sum_{i=1}^{n} I_{C,i}$$

$$V_{out} = V_{CC} - I_{RC} R_C$$



*All Inputs low:

If all inputs $< V_{BE(FA)}$ the all BJTs are cutoff. & $I_{RC} = 0$

$V_{OH} = V_{CC}$ (all inputs low)

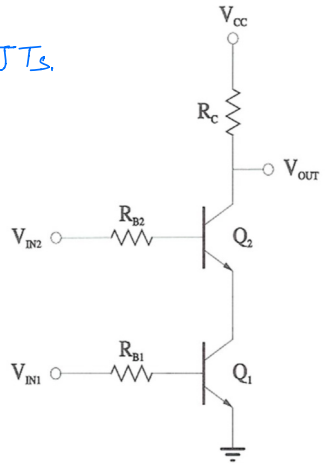
*Any Input High:

If any input $\geq V_{BE(FA)}$ the corresponding BJT conducts collector current and the resulting output is $< V_{CC}$.

If any input reaches V_{IH} the corresponding BJT enters saturation

$V_{OL} = V_{CE(sat)}$ (for input high)

Basic RTL NAND Gate.



* two-input RTL configuration with stacked BJTs.
* $\beta_f >> 1$ for both BJTs
* the base currents are negligible in comparison with the collector currents

$$I_{E1} \approx I_{C1}$$

$$I_{C1} \approx I_{E2}$$

$$\therefore I_{C1} = I_{C2} = I_{RC}$$

$$V_{out} = V_{CC} - I_{RC} R_C$$

* Any Input Low

If $V_{IN1} < V_{BE(FA)}$ then $I_{C1} = 0$

$\because I_{C1} = I_{C2} \Rightarrow \therefore I_{C2} = 0$

$\therefore Q_1$ is cutoff & therefore Q_2 is cutoff regardless of V_{IN2}

if V_{IN1} = high & V_{IN2} = low then $I_{C2} = I_{RC} = 0$ therefore if any input is low $I_{RC} = 0$

$$V_{OH} = V_{CC} \quad \text{(for any input low)}$$

* All Inputs High.

If V_{IN1} is high enough to saturate Q_1

$$V_{E2} = V_{C1} = V_{CE(sat)}$$

for Q_2 input to be FA its input V_{IN2} must then be at least

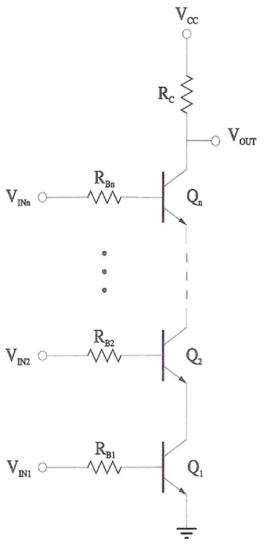
$$V_{IN2} = V_{BE2(FA)} + V_{CE1(sat)}$$

increase of V_2 means decrease of V_{out} & when Q_1 & Q_2 both saturated

$$V_{OL} = 2V_{CE(sat)} \quad \text{(both inputs high)}$$

Multi-Input RTL NAND Gate

$$V_{OL} = \sum_{i=1}^{n} V_{CE,i}(sat)$$



Example 5.1 ***Multi-Input RTL NAND Gate***

What is the maximum fan-in for the basic RTL NAND gate of Figure 5.4, if all stack BJTs have $V_{CE}(SAT) = 0.17$ V and all load gates have $V_{BE}(FA) = 0.7$ V?

$V_{CE}(sat) = 0.17V \quad V_{BE}(FA) = 0.7V$

the number of inputs is limited by:

$$n V_{CE}(sat) < V_{BE}(FA)$$

Note that V_{OL} must be low enough to maintain all load BJT in cut-off therefore the maximum number of inputs is:-

$$n < \frac{V_{BE}(FA)}{V_{CE}(sat)} = \frac{0.7}{0.17} = 9.12$$

$$\therefore n = 4$$

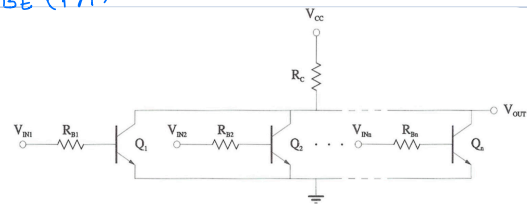
n= the maximum number of inputs

RTL Fan-Out

* When RTL gate such as NOR gate is in the output low state any load gate would be cut off and draw no input current because

$$V_{IN}' = V_{CE}(sat) < V_{BE}(FA)$$

$$N(low) = \frac{I_{out}(low)}{I_{IN}'(low)} = \frac{\square}{0} = \infty$$



$$N_{max} = \min(N_{high}, N_{low})$$

* When the driving gate in the output high state, all load gates are operating in saturation and draw input current.

* the maximum fan-out RTL gates is limited by the output high state, so the driving must supply enough driving current to saturate all load gates & this current must be supplied through R_C of the driving gate.

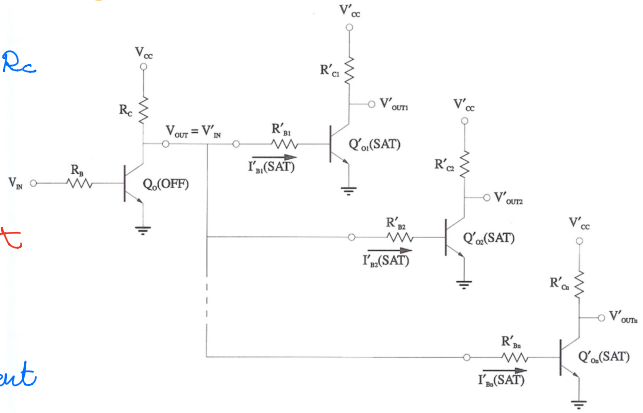
In the output high state a driving gate has an output high voltage degraded by the voltage drop across R_c

$$V_{OH} = V_{cc} - I_c R_c < V_{cc}$$

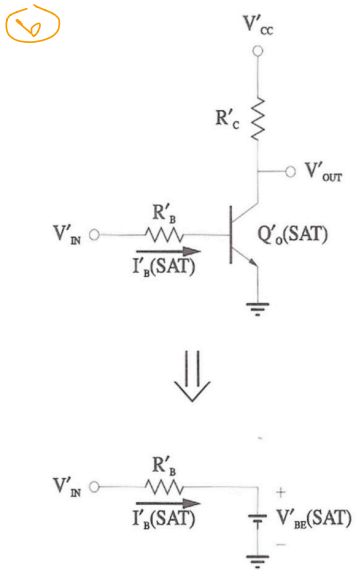
Development of Equivalent Circuit

* To solve for the maximum fan-out of an RTL gate it is convenient to develop an equivalent circuit for analysis

(a)



(b)



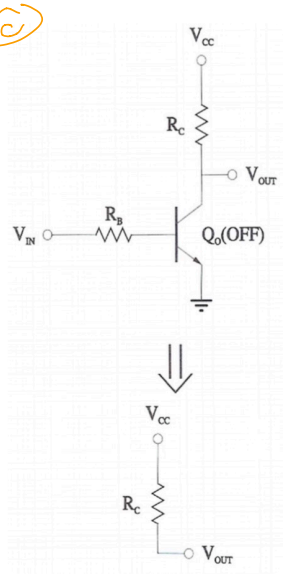
(f) $$I_{RC} = \sum_{i=1}^{n} I_N = N I'_B$$

$$\frac{V_{cc} - V_{out}}{R_c} = N\left(\frac{V_{out} - V_{BE(sat)}}{R'_B}\right)$$

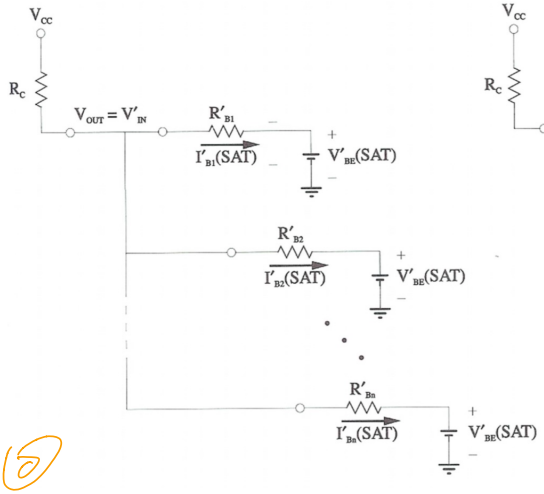
by solving for N & dropping the primes

$$N = \frac{V_{cc} - V_{out}}{V_{out} - V_{BE(sat)}}\left(\frac{R_B}{R_c}\right)$$

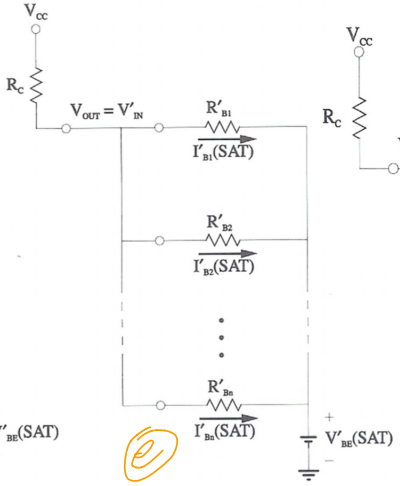
(c)



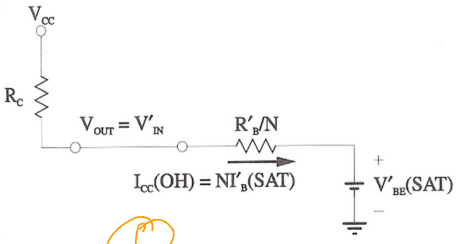
(d)



(e)



(f)



* the limiting factor in the maximum fan-out of the RTL inverter the V_{OH} of the driver gate must still be large enough to saturate the load gates

$$\therefore V_{OH(min)} = V_{IH}$$

$$V_{IH} = V'_{BE}(sat) + \left(\frac{V'_{cc} - V'_{CE}(sat)}{\beta_f R'_c}\right) R'_B$$

$$N = \frac{V_{cc} - V_{OH(min)}}{V_{OH(min)} - V_{BE(sat)}} \cdot \left(\frac{R_B}{R_c}\right)$$

Example 5.2 *Basic RTL Maximum Fan-Out*

What is the maximum fan-out for a basic RTL gate with $V_{CC} = 5$ V, $R_B = 10$ kΩ, and $R_C = 1$ kΩ? Let $\beta_F = 25$, $V_{BE}(SAT) = 0.8$ V, and $V_{CE}(SAT) = 0.2$ V.

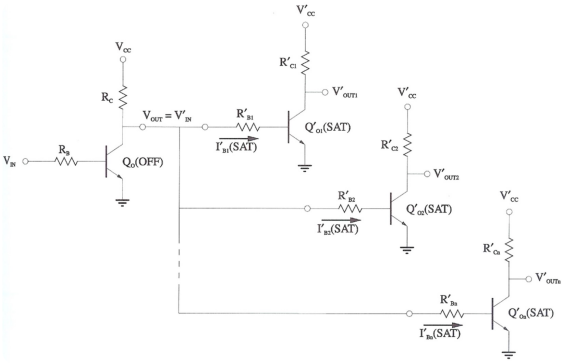
The minimum output high voltage.

$$V_{OH}(min) = V_{IH} = V_{BE(sat)} + \left(\frac{V_{cc} - V_{CE(sat)}}{\beta_f R_c}\right) R_B = 0.8 + \left(\frac{5 - 0.2}{25 \times 1K}\right)(10K) = 2.72\,V$$

$$N = \frac{V_{cc} - V_{out}}{V_{out} - V_{BE(sat)}}\left(\frac{R_B}{R_c}\right) = \frac{5 - 2.72}{2.72 - 0.8}\left(\frac{10K}{1K}\right) = 11.87$$

∴ the maximum fan-out is $N_{max} = 11$

RTL Power Dissipation



✳ Output Loco Current Supplied $\equiv I_{cc(OL)}$

$$V_{OL} = V_{CE}(sat) < V'_{BE}(FA)$$

$$I_{cc(OL)} = \frac{V_{cc} - V_{CE}(sat)}{R_c}$$

✳ Output High Current Supplied $\equiv I_{cc(OH)}$

For no load gates $I_{cc(OH)} = I_{C(off)} = 0$

$$I_{cc(OH)} = N I'_B(sat) = I_{RC}$$

$$= \frac{V_{cc} - V'_{BE}(sat)}{R_c + R'_B/N}$$

✳ Average Power Dissipation $\equiv P_{cc(avg)}$

$$P_{cc(avg)} = \left(\frac{I_{cc(OL)} + I_{cc(OH)}}{2}\right) V_{cc}$$

Example 5.3 ***RTL Power Dissipation***

Find the average power dissipated in a basic RTL inverter with

(a) no load

(b) a fan-out of 1

Use V_{CC} = 5 V, R_B = 10 kΩ, and R_C = 1 kΩ. Let β_F = 25, V_{BE}(SAT) = 0.8 V, and V_{CE}(SAT) = 0.2 V for the BJTs.

(a)

$$I_{CC(OL)} = \frac{V_{CC} - V_{CE(sat)}}{R_C} = \frac{5-0.2}{1k} = 4.8mA$$

$$I_{CC(OH)} = 0$$

$$P_{CC(avg)} = \frac{I_{CC(OH)} + I_{CC(OL)}}{2} V_{CC} = \frac{4.8m+0}{2} \times 5 = 12\ mW$$

(b) For a load gate $I_{CC(OL)}$ is unchanged but

$$I_{CC(OH)} = I_{IH} = \frac{V_{CC} - V_{BE(sat)}}{R_C + R'_B} = \frac{5-0.8}{1k+10k} = 382\mu A$$

$$P_{CC(avg)} = \frac{(4.8m)+(382\mu)}{2}(5) = 12.96\ mW$$

Basic RTL NON-INVERTER

* The basic RTL inverter can be modified to produce non-inverting output

$$V_{out} = V_E = I_E R_E = V_{CC} - V_{CE}$$

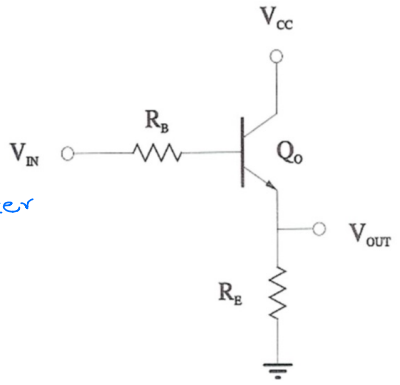
* Output Low Voltage ≡ V_{OL}

For $V_{IN} < V_{BE(FA)}$, the BJT in the non-inverter is cutoff

$$\Rightarrow I_C = I_{RE} = 0$$

$\Rightarrow$ there is no voltage drop across R_E

$$V_{out} = 0 = V_{OL}$$



* Input Low voltage $\equiv V_{IL}$

when V_{BE} reaches $V_{BE(FA)}$, the BJT enters the FA region

When V_{IN} is increased beyond $V_{BE(FA)}$ BJT terminal currents begin to conduct & the output voltage begins to increase.

$$V_{IL} = V_{BE(FA)}$$

* Output High Voltage $\equiv V_{OH}$

the non-inverter output can rise to only $V_{CE(sat)}$ below V_{CC}

$$V_{OH} = V_{CC} - V_{CE(sat)}$$

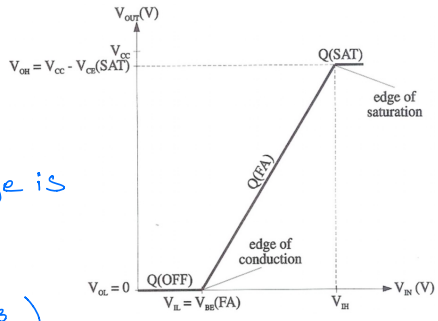
* Input High Voltage $\equiv V_{IH}$

The input high voltage is the minimum input necessary to saturate the BJT

$$I_{E(sat)} = \frac{V_{CC} - V_{CE(sat)}}{R_E}$$

at the edge of saturation $\alpha = 1$ and the base current is related to the emitter current by

$$I_{B(EOS)} = \frac{I_E}{\beta_f + 1} = \frac{V_{CC} - V_{CE(sat)}}{(\beta_f + 1) R_E}$$



with $V_{BC} = V_{BC(sat)}$ the input high voltage is

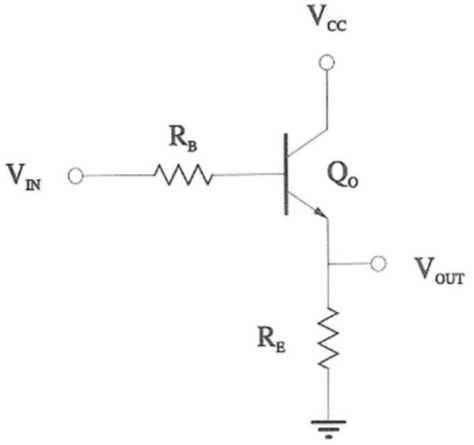
$$V_{IH} = V_{CC} + V_{BC(sat)} + I_{B(EOS)} R_B$$

$$= V_{CC} + V_{BC(sat)} + \frac{V_{CC} - V_{CE(sat)}}{(\beta_f + 1)} \left(\frac{R_B}{R_E} \right)$$

Note that V_{IH} for RTL non-inverter is greater than V_{CC} thus limiting its usage as a practical digital circuit.

Example 5.4 ***Basic RTL Non-inverter VTC***

Determine the critical voltages for the basic RTL noninverter in Figure 5.6 and show that V_{IH} is higher than V_{CC}. Use $V_{CC} = 5$ V, $R_B = 10$ kΩ, and $R_E = 1$ kΩ. Let $\beta_F = 25$, $V_{BE}(FA) = 0.7$ V, $V_{BE}(SAT) = 0.8$ V, and $V_{CE}(SAT) = 0.2$ for the BJT.



$V_{OL} = 0$

$V_{IL} = V_{BE(FA)} = 0.7\,V$

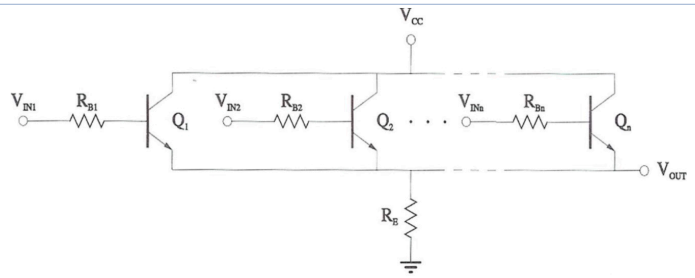
$V_{OH} = V_{CC} - V_{CE(sat)} = 5 - 0.2 = 4.8\,V$

$$V_{IH} = V_{CC} + V_{BE(sat)} + \frac{V_{CC} - V_{CE(sat)}}{(\beta_F + 1)} \left(\frac{R_B}{R_E}\right) = 5 + 0.6 + \frac{5 - 0.2}{25+1}\left(\frac{10K}{1K}\right) = 7.4V$$

the input high voltage of 7.4V is almost 50% higher than Vcc and is too high to be practical.

Basic RTL OR & AND Gates

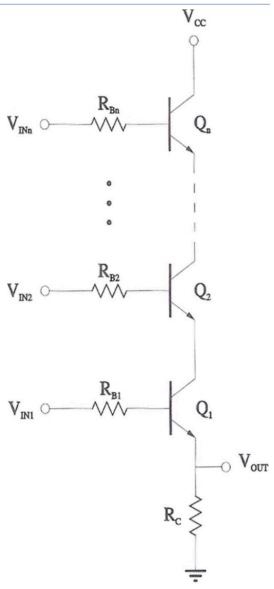
* Additional inputs can be added to the basic RTL non-inverter to form OR & AND gates



Basic RTL OR Gate

prove that ↑ work as OR gate

H.W → prove that → work as AND Gate



Basic RTL AND Gate

RTL with Active Pull-Up

* A method to increase the fan-out of RTL gates includes an active pull-up configuration.

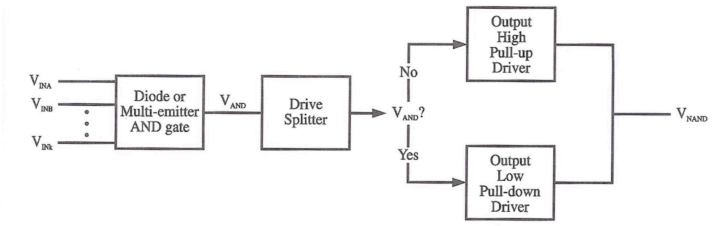


FIGURE 4.7 TTL Family Super-circuitry Block Diagram

* An RTL inverter using active pull-up is consists of Q_P, R_{BP} & R_{CP} & provides additional sourcing current in the output high state

* To accomplish active pull-up, R_{CP} is smaller than R_C by approximately one order of magnitude

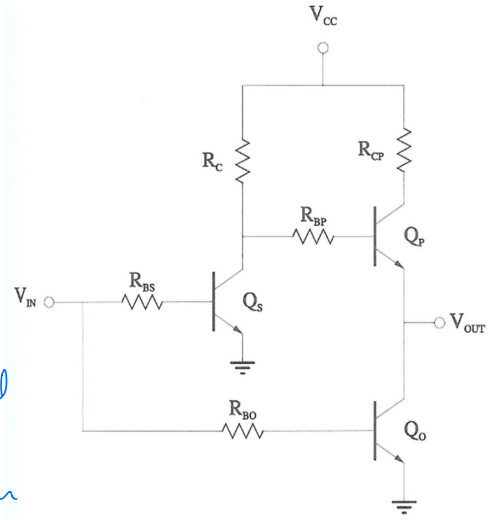


FIGURE 5.9 RTL Inverter with Active Pull-up

* Q_O operates as a BJT inverter and supplies active current sinking during the output low state.

* The magnitudes of R_{BS} & R_{BO} are equal so that Q_S & Q_O turn on and off simultaneously.

* The BJT Q_S operates as a BJT inverter & provides logic inversion to Q_P such that Q_P & Q_O are not on simultaneously.

TABLE 5.1 Purpose of Each Element for an RTL Gate with Active Pull-Up

Element	Purpose
R_{BS}, R_{BO}	Matched input resistors
Q_S	Drive splitter, pull-down of Q_P
R_C	Along with Q_S provides logic inversion to output-high driver
R_{BP}	Limits base current to Q_P
Q_O	Output inverting BJT, output-low driver for current sourcing pull-down
Q_P	Provides active current-sourcing pull-up
R_{CP}	Part of active pull-up

TABLE 5.2 States of BJTs for Output High and Low States

Element	V_{OH}	V_{OL}
Q_S	Cutoff	Saturated
Q_P	Saturated	Cutoff
Q_O	Cutoff	Saturated

* with the gate input high Q_S & Q_O are both saturated & we can examine $V_{BE,P}$ for a high input

$$V_{RBP} + V_{BE,P} = V_{CE,S}(sat) - V_{CE,O}(sat) = 0$$

Fan-Out of RTL with active Pull-Up

* the fan-out is limited by the current sourcing capability of the driving gate in the output high state

* In the output high state the driving gate will be connected to a low input

* Q_S & Q_O will be cut off & Q_P will be saturated

representation of the driving gate in the output high state

equivalent circuit for sing load gate with V_{IN} high

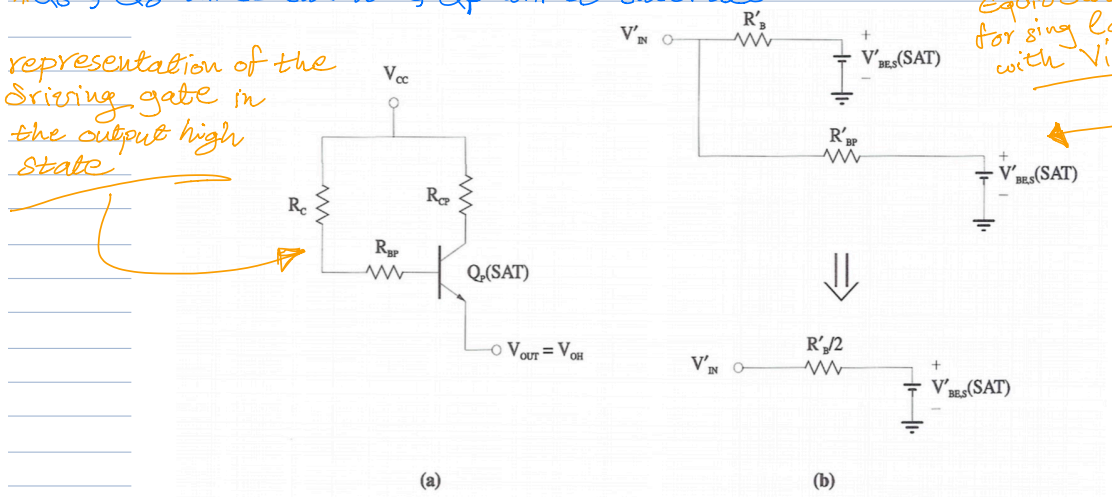
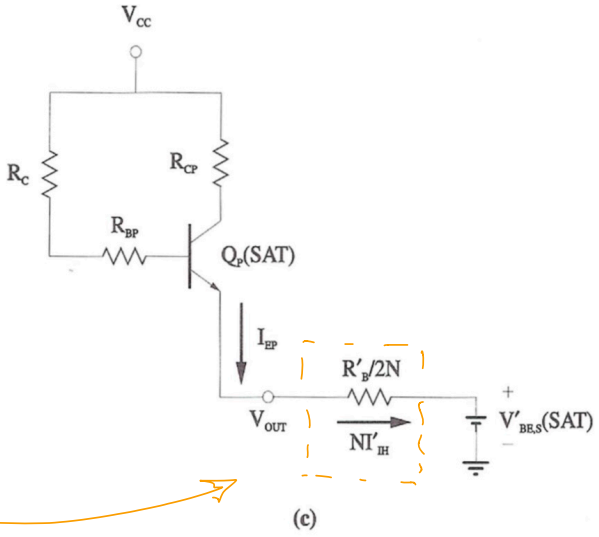


FIGURE 5.10 Development of Equivalent Circuit for Fan-out Calculation of RTL with Active Pull-up: (a) Equivalent circuit for output high state, (b) Equivalent circuit for input high

equivalent representation for a driving gate with N load gates

Note that a resistance of $R_B'/2N$ is present



(c) Circuit for fan-out calculation

$$I_{EP} = N I'_{IH}$$

assuming $I_{EP} \approx I_{CP}$

$$\frac{V_{CC} - V_{CE(sat)} - V_{out}}{R_{CP}} = \frac{V_{out} - V'_{BE(sat)}}{R'_B/2N}$$

$$N = \frac{V_{CC} - V_{CE(sat)} - V_{OUT}}{V_{OUT} - V'_{BE(sat)}} \left(\frac{R'_B}{2R_{CP}}\right)$$

* As the number of load gates is increased more current is sourced to the load gates through Q_P of the driving gate & the voltage drop across R_{CP} increases while V_{OH} decreases

* The limiting factor in the maximum fan-out of RTL with active pull-up is that the V_{out} of the driver gate must be large enough to saturate Q'_1 & Q'_2 of the load gates that means V_{OH} must be at least V_{IH}

$$V_{OH(min)} = V_{IH}$$

$$V_{OH(min)} = V_{BE(sat)} + \frac{V_{CC} - V_{CE(sat)}}{\beta_F R_C} R_B$$

$$N_{max} = \frac{V_{CC} - V_{CE(sat)} - V_{OH(min)}}{V_{OH(min)} - V_{BE(sat)}} \left(\frac{R_B}{2R_{CP}}\right)$$

Example 5.5 ***Maximum Fan-Out of RTL with Active Pull-Up***

Compare the maximum fan-out for the RTL inverter with active pull-up (shown in Figure 5.9) with that of basic RTL obtained in Example 5.2. Use the values of $V_{CC} = 5$ V, $R_{BP} = R_{BS} = R_{BO} = 10$ kΩ, $R_C = 1$ kΩ, $\beta_F = 25$, $V_{BE}(SAT) = 0.8$ V, and $V_{CE}(SAT) = 0.2$ V, which are the same values used in Example 5.2. Also, let $R_{CP} = 100$ Ω.

first we find the minimum V_{OH}

$$V_{OH(min)} = V_{IH} = V_{BE(sat)} + \frac{V_{cc} - V_{CE(sat)}}{\beta_f R_c} R_B$$

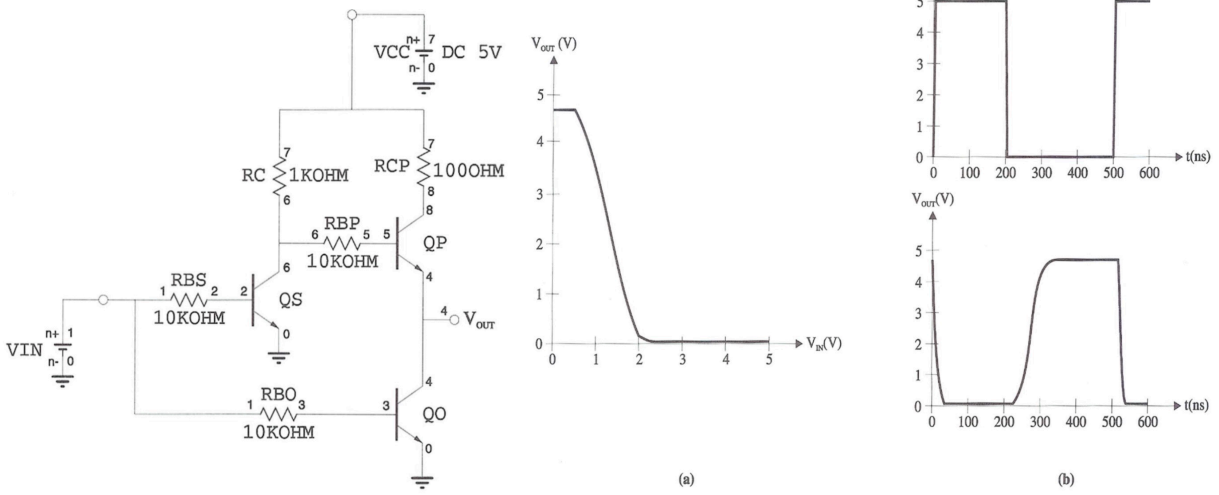
$$= 0.8 + \frac{5-0.2}{25\,(1K)}(10K) = 2.7V$$

$$N = \frac{V_{cc} - V_{CE(sat)} - V_{OH(min)}}{V_{OH(min)} - V_{BE(sat)}} \left(\frac{R_B}{2R_{CP}}\right)$$

$$= \left(\frac{5-0.2-2.7}{2.7-0.8}\right)\left(\frac{10K}{2(100)}\right) = 55.3$$

∴ The maximum fan-out for RTL with active pull-up is 55 an improvement of 500% as compared to the basic RTL fan-out.

RTL SPICE Simulation.



RTL with Active Pull-up and SPICE Labelings

FIGURE 5.12 Results of Section 5.9 SPICE Simulation of RTL Inverter with Active Pull-up: (a) Voltage transfer characteristic obtained from .DC sweep, (b) Transient response obtained from .TRAN sweep

Direct Coupled Transistor Logic & Current Hogging

* In an attempt to improve the packing density of RTL in IC form the base resistor R_B was eliminated.

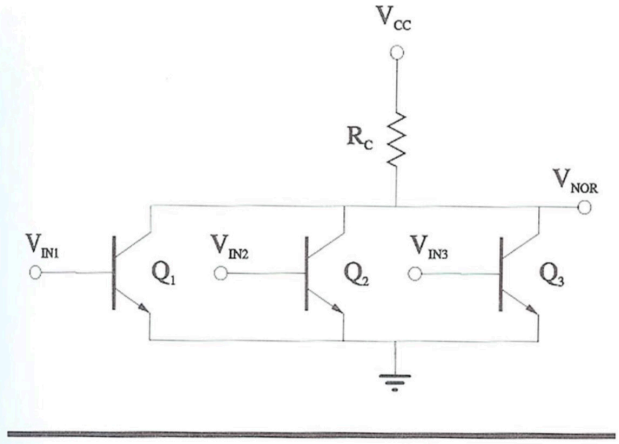


FIGURE 5.13 Three-input Direct Coupled Transistor Logic (DCTL) NOR Gate (no base resistors)

* The problem with DCTL occurs for $V_{out} = V_{OH}$ with fan-out greater than one because BJTs do not have exactly the same $V_{BE}(FA) = 0.7V$

* Since $R_B = 0$ the connected BJTs at the output have their J_{BE} directly in parallel. therefore the BJT with the smallest $V_{BE}(FA)$ will sink all of the current while the remaining BJTs are cutoff since each of these have $V_{BE} < V_{BE}(FA)$

Current Hogging

* the previous phenomena named current hogging because a single BJT hogs all of the current

* Current hogging is avoided by including bases or emitter resistors.

Example 5.6 ***DCTL Current Hogging***

Consider a direct-coupled RTL inverter without base resistors ($R_B = 0$). Also, let the fan-out be four and the connected BJTs have slightly different V_{BE}(FA) turn-on voltages given by 0.7 V, 0.7 V, 0.7 V, and 0.69 V. Determine the base current for each transistor and the output voltage of the inverter for the output high state (input low).

*An equivalent circuit to replace the inverter with a fan-out of four as shown on the figure to the right.

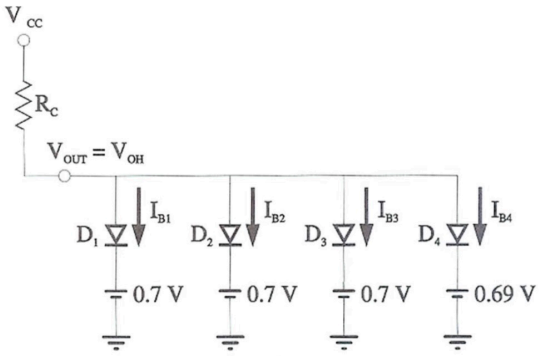


FIGURE 5.14 Equivalent Circuit for a DCTL Inverter in the Output High State with a Fan-out of Four for Example 5.5

*Each connected transistor base-to-emitter circuit has been replaced with a DC voltage & ideal diode.

*The BJT has been replaced with an open circuit since the input is low

*The ideal diode D_4 is the only diode that conducts currents because when D_4 shorts $V_{out} = 0.69V$ which is insufficient to short ideal diodes D_1, D_2 & D_3

* The base current of BJT 4 is

$$I_{B4} = \frac{V_{cc} - 0.69}{R_c}$$

*Note that BJT 4 hogs all the current & is the only transistor that conducts current therefor $I_{B1} = I_{B2} = I_{B3} = 0$ A.